

<b>Notice of References Cited</b>	Application/Control No. 10/078,180	Applicant(s)/Patent Under Reexamination MORROW, NEIL G.	
	Examiner Thomas J. Cleary	Art Unit 2111	Page 1 of 1

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*	B	US-6,070,214 A	05-2000	Ahern, Frank	710/315
	C	US-			
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	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

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**NON-PATENT DOCUMENTS**

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	U	"Free On-Line Dictionary of Computing", entry 'High Performance Serial Bus'. [posted 3 Sep 2000]. [retrieved 27 Apr 2004]. < <a href="http://foldoc.doc.ic.ac.uk/foldoc/foldoc.cgi?query=1394">http://foldoc.doc.ic.ac.uk/foldoc/foldoc.cgi?query=1394</a> >
	V	"Low Pin Count (LPC) Interface Specification", Revision 1.0 [29 Sep 1997]. Intel Corporation. Chapter 1, Page 1.
	W	"Time Budgeting of the FlatLink Interface", Application Report [June 1997]. Kevin Gingerich. Texas Instruments Incorporated.
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.